Semiconductors

AN10027_1

Interfacing the ISP1160x to NEC V832 Processor

January 2003

Application Note

Rev. 1.0

Revision History:

Version	Date	Descriptions	Author
1.0	January 2003	First release	Jason Ong

Note: ISP1160x denotes any Philips embedded USB host controller whose name starts with 'ISP1160'; this includes ISP1160A, ISP1160A1, and any future derivatives.

We welcome your feedback. Send it to wired.support@philips.com.

Philips Semiconductors - Asia Product Innovation Centre
Visit www.semiconductors.philips.com/buses/usb or www.flexiusb.com

PHILIPS

This is a legal agreement between you (either an individual or an entity) and Philips Semiconductors. By accepting this product, you indicate your agreement to the disclaimer specified as follows:

DISCLAIMER

PRODUCT IS DEEMED ACCEPTED BY RECIPIENT. THE PRODUCT IS PROVIDED “AS IS” WITHOUT WARRANTY OF ANY KIND. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, PHILIPS SEMICONDUCTORS FURTHER DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANT ABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NONINFRINGEMENT. THE ENTIRE RISK ARISING OUT OF THE USE OR PERFORMANCE OF THE PRODUCT AND DOCUMENTATION REMAINS WITH THE RECIPIENT. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, IN NO EVENT SHALL PHILIPS SEMICONDUCTORS OR ITS SUPPLIERS BE LIABLE FOR ANY CONSEQUENTIAL, INCIDENTAL, DIRECT, INDIRECT, SPECIAL, PUNITIVE, OR OTHER DAMAGES WHATSOEVER (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF BUSINESS PROFITS, BUSINESS INTERRUPTION, LOSS OF BUSINESS INFORMATION, OR OTHER PECUNIARY LOSS) ARISING OUT OF THIS AGREEMENT OR THE USE OF OR INABILITY TO USE THE PRODUCT, EVEN IF PHILIPS SEMICONDUCTORS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

CONTENTS

FIGURES

Note: ISP1160x denotes any Philips embedded USB host controller whose name starts with 'ISP1160'; this includes ISP1160A, ISP1160A1, and any future derivatives.

1. Overview

When ISP1160x is integrated into a personal digital assistant (PDA) or handheld personal computer (HPC), it is usually connected to the external bus interface of a Reduced Instruction Set Computer (RISC) processor. This application note deals with the critical issues in the ISP1160x embedded design, using the NEC V832 RISC processor as a concrete example.

2. ISP1160x Interface Signals to a RISC Processor Bus

The processor bus interface of ISP1160x is designed for a simple direct connection with a RISC processor. The data transfer can be done in the Programmed I/O (PIO) or direct memory access (DMA) mode. The estimated maximum data transfer rate on ISP1160x's generic processor bus is approximately 15 Mbyte/s. This is based on an ISP1160x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, ISP1160x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal Host Controller. The Host Controller uses 2 kbytes of the ping memory and 2 kbytes of the pong memory in its allocated memory.

The main ISP1160x signals to consider for connecting to the NEC V832 RISC processor are:

- A 16-bit data bus: (D[15:0]) for ISP1160x, which is "little endian" compatible.
- An address lines (A0) necessary for complete addressing of the ISP1160x internal registers:
  - **A0 = 0**—Selects the Data Port of the Host Controller
  - **A0 = 1**—Selects the Command Port of the Host Controller
- A $\overline{\text{CS}}$ line used to select ISP1160x in a certain address range of the host system. This input signal is active LOW.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are common read and write signals. These signals are active LOW.
- A DMA channel standard control lines: DREQ, $\overline{\text{DACK}}$ and EOT. These signals have programmable active levels.
- An interrupt line, which has programmable level/edge and polarity (active HIGH or LOW).
- The CLKOUT signal has a default power-on frequency of 12 MHz and the maximum value of 48 MHz.
- The $\overline{\text{RESET}}$ signal is active LOW.

3. NEC V832 (uPD705102)

This section highlights the main features of the NEC V832 processor of special interest for connecting to ISP1160x.

The NEC V832 processor divides its memory space into eight blocks, each having the following features that depend on the internal configuration settings:

- Bus size: 16 or 32 bits can be independently set for each area.
- Number of wait cycles can be independently set for each area. The total number of additional wait states inserted is equal to the biggest number of wait-states required by the READY signal or specified by the wait-state control bits (0 to 7 wait-states for blocks 1 through 4, and 7or 0 to 15 wait-states for blocks 5 and 6).
- Setting the type of space for each area will enable a direct connection to several possible types of memory: SRAM or ROM (blocks 1 through 7), SDRAM (block 0 and 1) and I/O (blocks 3 through 6).

- For correct data alignment, matching data width with endian is necessary. The ISP1160x connection will require a 16-bit/ little endian configuration of the selected memory area. The data bus width can be selected by setting the BWn (where n can take any value from 1 to 6) bit in the DBC register of NEC V832, and little endian corresponds to normal operation mode of V832.

ISP1160x can be connected as I/O (using IOWR#, IORD#, nBEN# and CSn#, where n can take any value from 3 to 6) or SRAM (using MWR#, MRD#, nBEN#, CSn#, where n can take any value from 1 to 6).

4. Considerations in Timing Diagrams and WAIT States

This section presents a short study of the timing diagrams of the main bus cycles of both ISP1160x and NEC V832.

According to the ISP1160x datasheet specifications, a read cycle requires the following main timing parameters (the requirements of the write cycle is similar):

- t_{RL} = 33 ns ($\overline{RD}$ LOW pulse width—minimal value required by ISP1160x),
- t_{RHRL} = 110 ns ($\overline{RD}$ HIGH to next $\overline{RD}$ LOW—minimal value required by ISP1160x) and
- t_{RHDZ} = 3 ns ($\overline{RD}$ hold time, minimal value that can be expected from ISP1160x).
- t_{RC} = 143 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SHSL} = 300 ns (first $\overline{RD}$/ $\overline{WR}$ after command).

For a detailed analysis of the timing diagram, consider the access of an ISP1160x internal register (for example, the Control Register of the Host Controller). This requires two phases: writing the address of the selected register into the Command Port; and then only data transfer access ($\overline{RD}$/ $\overline{WR}$) may take place.

The timing diagram in Figure 4-1 describes the two phases of accessing ISP1160x:

- The first phase is accessing the Command (control) Port of ISP1160x, to write the address (index) of the data port that will be accessed. In this phase $\overline{CS}$ is active, the data lines D[15:0] contain the desired address. The $\overline{WR}$ pulse will be activated and will latch the data. Note the value of t_{SHSL} that represents the minimum time required between occurrence of the first phase and the second phase. As an example of the Host Controller "Control Register" a value of 01H will be transferred during an $\overline{RD}$ operation and 81H during a $\overline{WR}$ operation.
- The second phase consists of the access (read or write) to the data port selected by the address latched in the previous phase. Two timing diagrams are combined again in this second phase: one for the read access and one for the write access. A series of $\overline{RD}$ and $\overline{WR}$ pulses are shown in the diagram to define the timing requirements between two consecutive accesses to ISP1160x: t_{RHRL}, t_{WHWL}, t_{RC}, t_{WC}, t_{RLDV}, as specified in the datasheet.

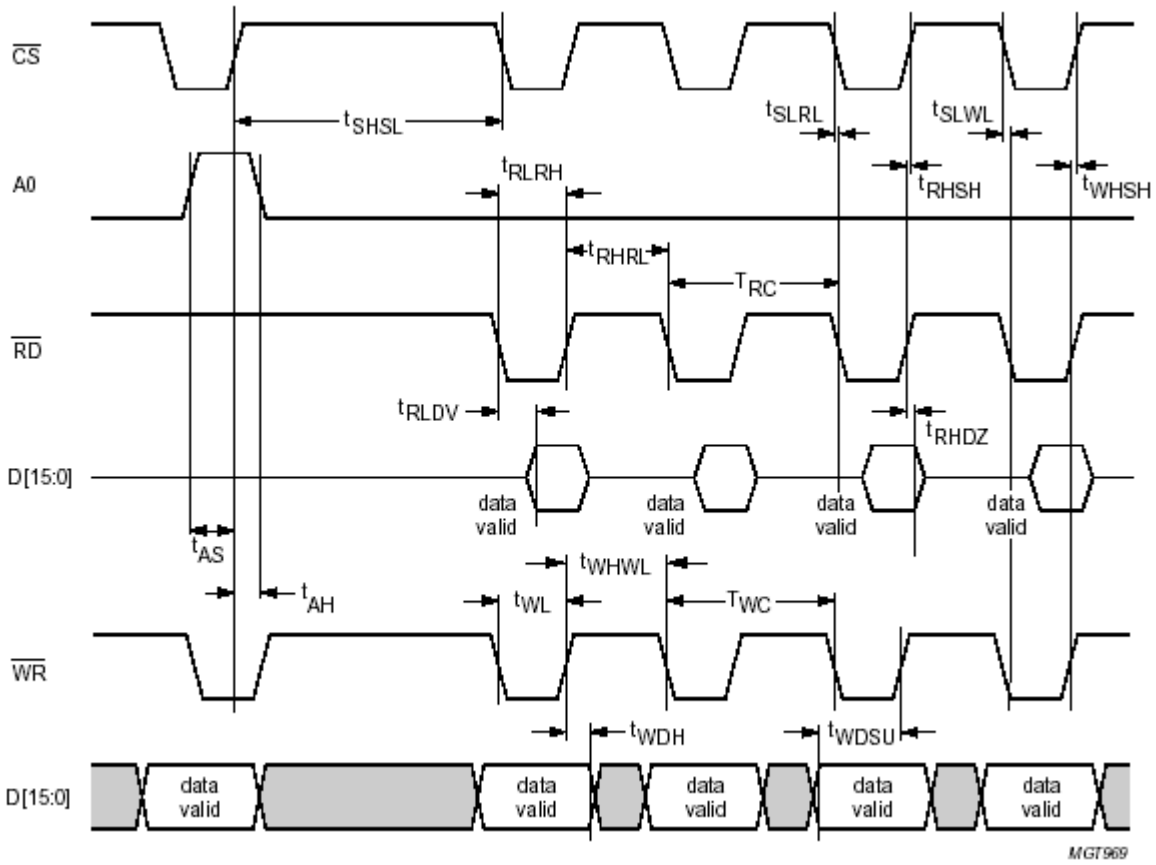


Figure 4-1: Programmed Interface Timing (16-bit Read/Write)

When the connection area of ISP1160x is defined as SRAM, ISP1160x will operate correctly for a bus clock CKIO = 33 MHz. Timing measurements show that insertion of wait-states in the standard bus cycles of the NEC V832 is not necessary. Nevertheless, we will describe wait-state insertion, to cater for cases when faster bus cycles are used for accessing ISP1160x.

Wait states insertion can be implemented by hardware or software. Both solutions will delay the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next CKIO cycle and will determine an elongation of the $\overline{RD}$ or $\overline{WR}$ LOW pulse that can be calculated as:

t_w = W x T(CKIO); where: (W) is the number of wait states desired.

T(CKIO) is the cycle length of CKIO.

Note: the value of t_{RHRL} will not be modified by the number of wait states inserted by any of the solutions mentioned earlier. The value of this parameter must be calculated and correctly adjusted according to the number and length of instructions executed by the NEC V832 processor between two successive accesses to ISP1160x. The "software solution" for wait-state insertion in a bus cycle is simple and is preferred in a minimal configuration, if additional wait states are necessary.

5. Using interrupts

ISP1160x generates an interrupt on the INT pin. ISP1160x's INT can be programmed as active on level or edge and HIGH or LOW, as specified in the *HcHardwareConfiguration* Register of the Host Controller.

6. DMA Operation

The ISP1160x DMA handlers can work in the DACK mode or in the 8237 mode by using the EOT (End Of Transfer) signal, according to the bits setting of the *Hardware Control* registers. To define the parameters of the DMA operation (transfer counter enable, DMA enable, burst length), you must program the *HcDMAConfiguration* and *HcTransferCounter* registers. Details on programming of DMA registers can be found in the ISP1160x datasheet and the *ISP1160x Embedded Programming Guide*.

Connection of ISP1160x's DMA channel signals to V832 can be achieved by connecting ISP1160x's DREQ and $\overline{\text{DACK}}$ signals to V832's DMARQ0 and DMAAK0 signals, respectively, because of the flexible interfaces of both ISP1160x and the NEC processor. In this configuration, connect ISP1160x's EOT signal to NEC V832's TC# input pin.

As shown in the following timing diagram, by asserting the DACK signal, the host system allows data to be transferred, allocating the bus for ISP1160x. Both the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ data transfer cycles are contained in the timing diagram. The $\overline{\text{CS}}$ signal is not used by the internal selection logic of ISP1160x, and the DMAAK1 and DMAAK2 signals are used to define the bus owner that issued DREQ and is currently involved in the data transfer. No other system resource on the same bus will be accessed as long as the DMA cycle is in progress and occupies the bus. The series of DMAAK1 or DMAAK2 active pulses determine the time allocated to the DMA data transfer.

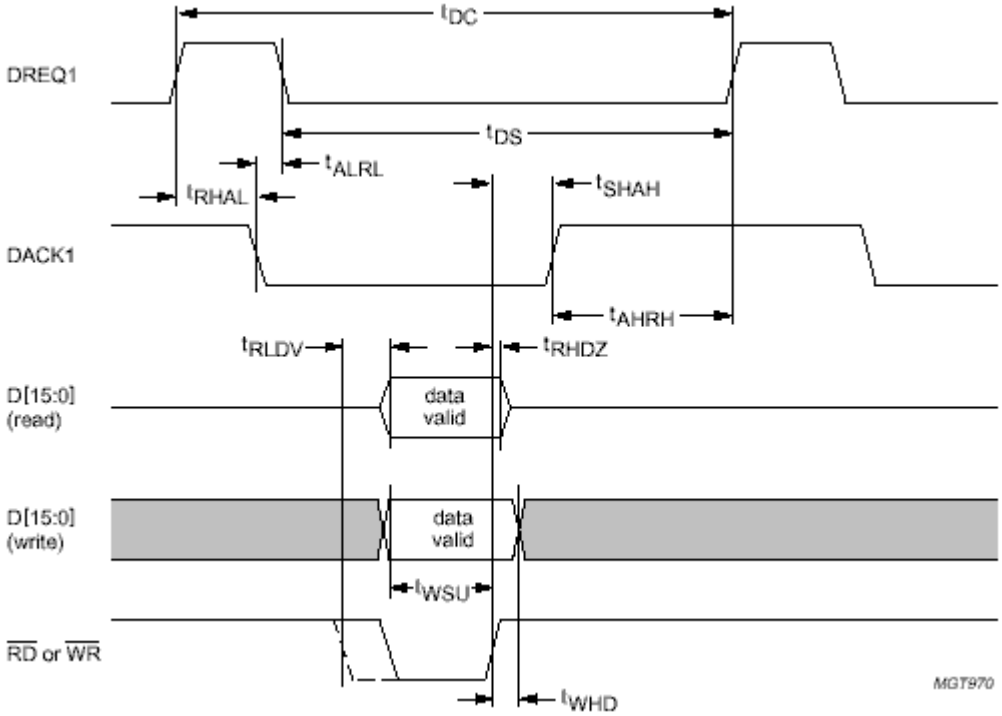


Figure 6-1: Host Controller Single-Cycle DMA Timing

A DMA burst access of up to 8 cycles for the ISP1160x host DMA handler can be defined in the *HcDMAConfiguration* Register.

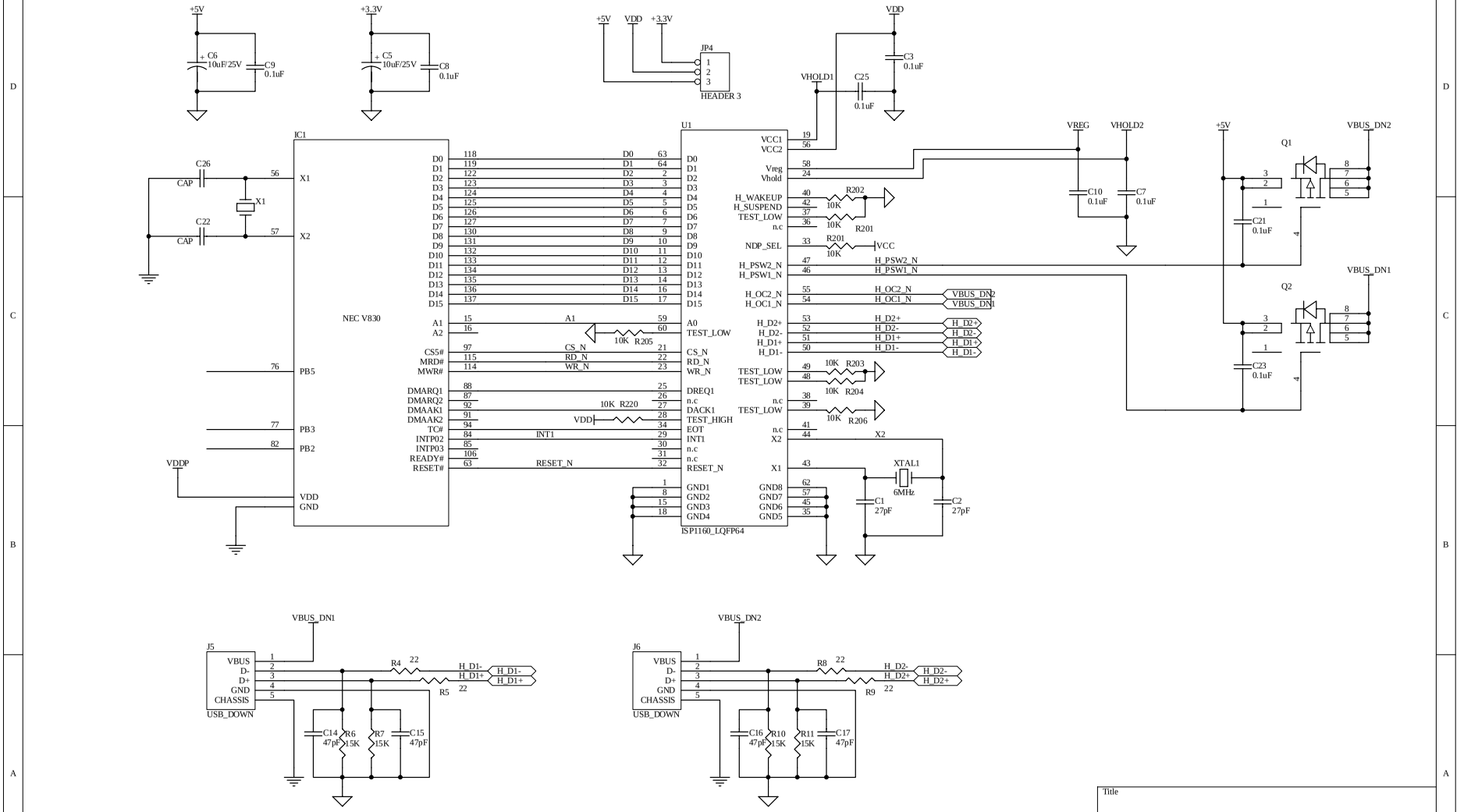
If necessary, add wait states to the basic DMA cycle to create longer $\overline{\text{RD}}$/$\overline{\text{WR}}$ and DMAAK pulses. To learn how to insert wait states, see Section 4.

7. Schematic Diagram

The following schematic diagram shows ISP1160x connected to the NEC V832 processor, in a minimal hardware configuration.

In this example schematic, ISP1160x is simply selected by CS5# (in a more complex configuration some glue logic may be required to generate a CS signal composed of CSn and several address lines).

ISP1160x uses the input signals $\overline{H\_OC1}$ and $\overline{H\_OC2}$ to detect an overcurrent on the downstream ports. Because separate overcurrent detection and protection circuits are implemented for each ISP1160x downstream facing port, so when an overcurrent is detected on a downstream facing port, power will be turned off to that port only. Connecting the voltages of the two downstream ports VBUS_DN1 and VBUS_DN2 to the $\overline{H\_OC1}$ and $\overline{H\_OC2}$ pins enables current value to be detected by sensing the voltage drop on Q1 and Q2 that are PMOS transistors with very low switch-on resistance Rds(on). Selection between Q1 and Q2 depends on the desired maximum current value and this determines the value of Rds(on). For example, if the allowed maximum current is approximately 0.5 A, a voltage drop of 75 mV will trigger the overcurrent circuitry and Rds(on) of approximately 150 MΩ will result. Connecting the ISP1160x input pins $\overline{H\_OC1}$ and $\overline{H\_OC2}$ to +5 V will disable ISP1160x's internal overcurrent protection. You can opt for an external overcurrent protection circuit.



Title		
Size: B	Number:	Revision:
Date: 27-Dec-2002		Sheet of
File: I:\Jason Backup 030701\Philips\ISP1161\Documentation\App Note Schematic\1160 NEC.DDB		Drawn By:

8. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1160 Embedded Universal Serial Bus Host Controller* datasheet
- *ISP1160A1 Embedded Universal Serial Bus Host Controller* datasheet
- *Interfacing ISP1160x to Hitachi SH7709 RISC Processor* application note

Philips Semiconductors

Philips Semiconductors is a worldwide company with over 100 sales offices in more than 50 countries. For a complete up-to-date list of our sales offices please e-mail sales.addresses@www.semiconductors.philips.com.
A complete list will be sent to you automatically.
You can also visit our website
http://www.semiconductors.philips.com/sales/

www.semiconductors.philips.com

PHILIPS